REMARKS

In response to the final Office Action mailed June 27, 2005, applicant respectfully requests reconsideration and entrance of the foregoing amendments. In the Office Action, claims 1-24 were rejected. By this amendment, amendments to claims 9 and 21 have been proposed. Claims 1-24 remain pending in the application.

Objection to Claims

Claims 9 and 21 were objected to because of various informalities stated in the previous Office Action. Regarding claims 9 and 21, the examiner states that it is not clear how the second logic section may be used in causing the memory to store an erroneous value. Claims 9 and 21 have been amended to make the operation of the second logic section more clear.

Rejections Under 35 U.S.C. §112

Claims 9 and 21 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite.

As set forth above, claims 9 and 21 have been amended to make the operation of the second logic section more clear, thereby rendering this rejection moot.

Claim Rejections Under 35 U.S.C. §103

Claims 1-24 remain rejected under 35 U.S.C. §103(a) as being unpatentable over Irrinki et al. in view of Lattimore et al.

The examiner incorporated his points into a single argument, so the applicant will address the argument as it applies to all of the independent claims and not specifically with regard to each independent claim.

Irrinki teaches a method for testing memory devices during the manufacturing process (Col. 1, lines 10-11). The method includes using BIST 120 for testing for faulty memory cells in an associated memory array 140 during power-up. Upon power-up, BIST unit 120 cycles memory array 140 through various test patterns. Every time a failing row or column is detected by the BIST 120, the information is conveyed to the

BISR 110 which attempts to reassign accesses to the failing location to a redundant row or column within the array (Col. 3, lines 58-63). However, the BIST 120 only operates at power-up (Col. 4, lines 6-7; Col. 6, lines 35-36; Col. 7, lines 43-45). When power is applied to memory storage device 100, BIST 120 begins a test algorithm to verify the operation of memory array 140 (Col. 5, lines 20-22). After the BIST 120 has completed its testing, state machine controller 210 of BIST 120 becomes inactive and stops asserting BIST select signal 124. After this occurs, normal operation of the memory array proceeds and address 132 is selected at address multiplexer 250 (Col. 5, lines 52-62). BISR 110 monitors incoming addresses on uncorrected address line 116 to determine if any match one of the failing addresses detected by the BIST 120. If a match is found, BISR 110 conveys the corrected address 114 using corrected address select signal 112 through multiplexer 252 (Col. 3, line 63- col. 4, line 5).

In response to applicant's argument that (a) there is no motivation for the addition of Lattimore's bus interface unit or CPU to Irrinki's multiplexer 250, nor is there motivation for the signals from the external pins to be "controlled" during normal operation; and (b) the combination suggested by the examiner is improper as not being supported by any motivation to combine in either reference, the examiner states that it is not necessary that the references actually suggest, expressly or in so many words, the changes or improvements that applicant has made. The examiner further states that "[t]he test for combining references is what the references as a whole would have suggested to one of ordinary skill in the art."

In establishing a *prima facia* case of obviousness under 35 USC 103, it is incumbent upon the Examiner to provide a "clear and particular" showing of "actual evidence" of a suggestion, teaching, or motivation to combine references. In re Dembiczak, 50 USPQ 2d, 1614, 1617 (Fed. Cir. 1999). "Broad conclusory statements regarding the teachings of multiple references, standing alone, are not evidence." Id., citing McElmury v. Arkansas Power and Light Co., 995 F.2d 1576, 1578, 27 USPQ2d. 1129, 1131 (Fed. Cir. 1993) (internal quotations omitted).

In fact, in In re Dembiczak the Court of Appeals for the Federal Circuit recognized that "rigorous application" of the requirement for a showing of a teaching or motivation to combine references is the "best defense against the subtle but powerful

attraction" of improper hindsight-based obvious analysis. Id.; See also, Para-Ordnance Manufacturing, Inc. v. SGS Importers International, Inc., 73 F.3d 1085, 37 USPQ2d 1237 (Fed. Cir. 1995). ("obviousness may not be established using hindsight or in view of the teachings or suggestions of the inventor"). This is especially true in cases where the ease with which the invention may be understood "may prompt one to fall victim to the insidious effect of hindsight syndrome wherein that which only the inventor taught is used against its teacher." Id. citing W.L. Gore & Assoc., Inc. v. Garlock, Inc., 721 F.2d 1540, 1553, 220 USPQ 303, 313 (Fed. Cir. 1983).

Applicant maintains that there is no motivation for the modification suggested by the examiner and that the modification is therefore improper. As stated in applicant's previous response, there is no need for Irrinki to "control" signals from the external pins during normal operation. Once the BIST 120 becomes inactive, as described above, the memory device operated normally and the external signals are input through the control block 130 and to the memory array 140, as described above. Accordingly, since Irrinki does not need to control signals from external pins during normal operation, there is no suggestion, explicit, implicit or otherwise, to modify Irrinki as suggested by the examiner to incorporate a feature of Lattimore to provide this control function. Therefore, the "references as a whole" would not have suggested such a modification to one of ordinary skill in the art.

Furthermore, the examiner has not pointed out even an implied suggestion in Irrinki of the modification proposed by the examiner or any indication that such a modification would be desirable in Irrinki's system. Applicant asserts that this is because, absent applicant's disclosure, there is no support for such a modification. The examiner cannot use applicant's disclosure as a template for piecing together various references that separately might teach different elements of the claimed invention, without showing some suggestion from the references to support the combination. Moreover, the examiner cannot rely on general statements from case law about tests for combining references to justify a combination of references without pointing out the motivation in the references. In this case, the applicant has provided specific support for the assertion that there is no motivation to combine the references: there is no need for Irrinki to "control" signals from the external pins during normal operation. Once the

BIST 120 becomes inactive, as described above, the memory device is operated normally and the external signals are input through the control block 130 and to the memory array 140. Since, during normal operation, the BIST 120 becomes inactive, applicant asserts that Irrinki not only doesn't suggest the modification proposed by the examiner, but actually teaches against it. Would one of ordinary skill in the art be motivated to modify an element of Irrinki to perform a function even though the element is inactive and the performance of that function is not necessary or desired? Applicant believes that he/she would not.

Accordingly, because the combination suggested by the examiner is improper as not being supported by any motivation to combine in either reference, the rejection of claims 1-24 under 35 U.S.C. §103(a) is improper and should be withdrawn.

Furthermore, even if the combination were proper, which applicant asserts that it is not, the combination would not teach the invention recited in claims 1-24. Independent claim 1 recites a testing system for use in testing a system-under-test (SUT), the testing system comprising:

a first logic section that may transmit one or more test-related signals for use during a test mode of the SUT;

a second logic section that may transmit one or more other signals during a normal operating mode of the SUT; and

a third logic section that selectively couples the first logic section or the second logic section to the SUT based upon respective assertion states of two control signals, one of the two control signals being transmitted to the third logic section from a source that is external to the SUT, the first logic section, the second logic section, and the third logic section, the other of the two control signals being transmitted to the third logic section from the first logic section;

wherein:

> when the third logic section couples the first logic section to the SUT, the first logic section transmits the one or more test-related signals to the SUT, and when the third logic section couples the second logic section to the SUT, the second logic section may transmit the one or more other signals to the SUT.

In response to applicant's argument that Irrinki does not teach a first logic section, a second logic section and a third logic section since the multiplexers 250, 252 that the examiner states correspond to the third logic section in the claim are actually part of the control block 130, which the examiner states corresponds to the second logic section, the examiner argues that it would be obvious to relocate the multiplexers into a third logic section. Applicant disagrees with the examiner's position.

As shown in Fig. 1, Uncorrected Address signal 116 is output from the Control Block 130 to the BISR 110. Likewise, the Corrected Address Select signal 112 is output from the BISR 112 to the Control Block 130. As further shown in Fig. 2, the Uncorrected Address signal 116 is output from the multiplexer 250 and the Corrected Address Select signal is input to the multiplexer 252. Accordingly, the multiplexers 250 and 252 are part of the Control Block 130, which the examiner has stated corresponds to applicant's second logic section. If the multiplexers 250 and 252 are part of what the examiner is calling the second logic section, they cannot also be part of a third logic section, and they certainly do not selectively couple the first logic section or the second logic section to the SUT.

Fig. 2 shows the Control Block 130, which comprises multiplexers 250, 252, 254 and 256, the BIST 120 and the memory Array 140. The examiner states that it would have been obvious to relocate the multiplexers 250 and 252 into a third logic section. First, such a "relocation" could only happen based on hindsight reconstruction, as one of ordinary skill in the art would have absolutely no motivation to contradict the teachings of Irrinki that the multiplexers 250 and 252 are part of the Control Block 130 along with multiplexers 254 and 256 without going backwards from applicant's disclosure. Second, even if the modification were proper, it would not show what is recited in the independent claims, specifically that the third logic section (multiplexers 250 and 252 according to the examiner) selectively couples the first logic section or the second logic section to the SUT. Based on the examiner's reasoning that the multiplexers 250 and 252 are the third logic section, then the multiplexers 254 and 256, which are the remaining components of the Control Block 130, must be the second logic section. However, the multiplexers 250 and 252 have no connection to, or control over the multiplexers 254 and

256. Accordingly, multiplexers 250 and 252 (the third logic section according to the examiner) do not and cannot selectively couple the first logic section (BIST 120 according to the examiner) or the second logic section (multiplexers 254 and 256 according to the examiner) to the SUT (memory array 140 according to the examiner). Multiplexer 254 is coupled to the array 140 by Array Write Enable line 244 and multiplexer 256 is coupled to array 140 by Array Data In line 246 at all times and regardless of the operation of the multiplexers 250 and 252. BIST 120 is coupled to array 140 by Data Out line 138 at all times and regardless of the operation of the multiplexers 250 and 252. Accordingly, the multiplexers 250 and 252 (the third logic section according to the examiner) do not selectively couple the first or the section logic sections to the SUT as is recited in the independent claims.

In response to applicant's argument that Irrinki does not teach two control signals, the examiner states that Irrinki teaches a first control signal, the BIST Select 124, and a second control signal, the Corrected Address Select 112. However, as recited in claim 1, the third logic section selectively couples the first logic section or the second logic section to the SUT based on the respective assertion states of two control signals. Since, as set forth above, Irrinki, nor the combination of Irrinki and Lattimore, do not teach a third logic section that selectively couples the first logic section or the second logic section to the SUT, the signals upon which such a selection is based are irrelevant.

Accordingly, since the (improper) combination of Irrinki and Lattimore does not teach or suggest the invention recited in the independent claims, applicant asserts that independent claims 1, 10, 13 and 22 are allowable over the combination, and the rejection of independent claim 1 under 35 U.S.C. §103(a) should be withdrawn.

Claims 2-9, 11, 12, 14-21, 23 and 24 depend from their respective independent claims and are allowable for at least the same reasons as the independent claims.

Based on the foregoing, applicants respectfully assert that claims 1-24 are allowable over the art of record and respectfully request that a timely Notice of Allowance be issued in this application.

In the event the Patent Office deems personal contact desirable in disposition of this matter, the Office is invited to contact the undersigned attorney at (508) 293-7835.

Please charge any fees occasioned by this submission to Deposit Account No. 05-0889.

Respectfully submitted,

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